

What is Claimed is:

- [c1] A circuit for controlling a memory cell, said circuit comprising:
 - a write driver having an output for operable applying an output signal at the memory cell; and wherein the write driver has a first and second and selectable operating modes, the first mode setting the write driver to apply a weak write output signal for performing a weak write test on the cell, the second mode setting the write driver to apply a write output signal that is sufficiently strong for writing a data value into the cell when it is healthy; and a write margin test circuit which increases sensitivity to resistive defects.
- [c2] The circuit of claim 1 wherein the write margin test circuit blocks a bitline restore driver.
- [c3] The circuit of claim 2 wherein the write margin test circuit includes a NAND gate connected to the bitline restore driver .
- [c4] The circuit of claim 3 wherein the write margin test circuit is activated by a write margin test signal.
- [c5] The circuit of claim 4 wherein at least two transistors are used to force a bit line restore signal high during the write margin test.
- [c6] The circuit of claim 5 wherein cells are identified if they fail the write margin test.
- [c7] The circuit of claim 6 wherein the identified failed cells are replaced with redundant memory elements.
- [c8] An active restore circuit for write margin testing of an SRAM having a bitline restore driver comprising:
 - a NAND gate connected to the bitline restore driver having three terminals;
 - a write margin test signal is applied to the first NAND gate terminal to activate the margin test;
 - a sub array clock signal (COLSEC) is applied to the second terminal of the

NAND gate which generates a restore signal to the bitline restore driver to block the bitline restore devices from turning off during the SRAM write cycle.

- [c9] The circuit of claim 8 which includes two transistors in the bitline restore driver to assist the bitline driver to block the bitline restore devices from turning off.
- [c10] The circuit of claim 9 wherein cells are identified if they fail the write test margin test.
- [c11] The circuit of claim 10 wherein the identified failed cells are replaced with redundant memory elements.